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PATENT APPLICATION

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1/17/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

IINUMA et al.

ATTN: Application Branch

Application No.: 09/857,184

Attorney Dkt. No.: 101201-00021

Filed: June 19, 2001

For: DIVERSITY RECEIVING APPARATUS THAT PREVENTS JUDGMENT  
ERRORS DURING DECODING AND A CLOCK GENERATING CIRCUIT FOR  
A DIVERSITY CIRCUIT THAT PREVENTS JUDGMENT ERRORS DURING  
DECODING

**REQUEST FOR CORRECTED FILING RECEIPT**

Commissioner for Patents  
Washington, D.C. 20231

September 18, 2001

Sir:

A corrected filing receipt is hereby requested.

Please change the Title from "**DIVERSITY RECEIVER FREE FROM  
DECODING ERROR, AND CLOCK REGENERATION CIRCUIT FOR DIVERSITY  
RECEIVER**" to **--DIVERSITY RECEIVING APPARATUS THAT PREVENTS  
JUDGMENT ERRORS DURING DECODING AND A CLOCK GENERATING  
CIRCUIT FOR A DIVERSITY CIRCUIT THAT PREVENTS JUDGMENT ERRORS  
DURING DECODING--**

For the convenience of the Patent and Trademark Office, attached is a  
photocopy of the original filing receipt on which the errors have been noted in red.

Please charge any deficiency or credit any overpayment with respect to this  
paper to Deposit Account No. 01-2300.

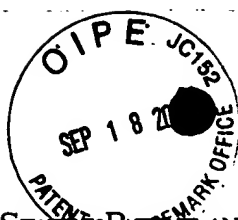
Respectfully submitted,

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DTN/baw



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COMMISSIONER FOR PATENTS  
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| APPLICATION NUMBER | FILING DATE | GRP ART UNIT | FIL FEE REC'D | ATTY. DOCKET NO | DRAWINGS | TOT CLAIMS | IND CLAIMS |
|--------------------|-------------|--------------|---------------|-----------------|----------|------------|------------|
| 09/857,184         | 06/19/2001  | 2682         | 940           | P101201-0002    | 8        | 13         | 4          |

CONFIRMATION NO. 9104

4372

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WASHINGTON, DC 20036

## FILING RECEIPT



\*OC00000006341058\*

Date Mailed: 07/25/2001

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## Applicant(s)

Toshinori Iinuma, Osaka, JAPAN;

## Domestic Priority data as claimed by applicant

THIS APPLICATION IS A 371 OF PCT/JP98/05941 12/25/1998

## Foreign Applications

Projected Publication Date: N/A

Non-Publication Request: No

Early Publication Request: No

## Title

Diversity receiver free from decoding error, and clock regeneration circuit for diversity receiver

## Preliminary Class

Diversity receiving apparatus that prevents judgment errors during decoding and a clock generating circuit for a diversity circuit that prevents judgement errors during decoding

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Data entry by : NGUYEN, SON

Team : OIPE

Date: 07/25/2001

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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